

## REMARKS

Claims 1-12 stand rejected. Reconsideration of the application is respectfully requested.

### Rejections Under 35 U.S.C. § 112

The Examiner rejected claim 12 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicants respectfully traverse this rejection.

The Court of Appeals for the Federal Circuit has repeatedly addressed the issue of sufficiency of disclosure, and that Court's precedent controls in these issues. Moreover, the standard for determining whether the specification meets the enablement requirement was cast in the Supreme Court decision of *Mineral Separation v. Hyde*, 242 U.S. 261, 270 (1916) in terms of the degree of experimentation needed to practice the claimed invention, and whether this degree of experimentation is undue or unreasonable. The Federal Circuit continues to employ this same standard. *In re Wands*, 8 U.S.P.Q.2d 1400, 1404 (Fed. Cir. 1998). A patent need not teach, and preferably omits, what is well known in the art. *In re Buchner*, 18 U.S.P.Q.2d 1331, 1332 (Fed. Cir. 1991). Moreover, it has long been settled that so long as the specification discloses at least one method for making and using the claimed invention that bears a reasonable correlation to the entire scope of the claims, the enablement requirement under 35 U.S.C. § 112 is satisfied. *In re Fisher*, 166 U.S.P.Q. 18, 24 (C.C.P.A. 1970). The Examiner bears the burden of establishing a *prima facie* case of non-enablement. A specification disclosure which contains a teaching of the

manner and process of making and using a claimed invention in terms which correspond to the scope of those used in describing and defining the subject matter sought to be patented, must be taken as being in compliance with the enablement requirement. M.P.E.P. § 2164.04.

Applicants respectfully submit that the terms recited in the claims are clearly described in the specification in such a way as to enable one skilled in the art to make and/or use the claimed invention and that the Examiner has not proven otherwise in any event. Specifically, with regard to the Examiner's rejection of claim 12, Applicants respectfully submit that the term "tri-state" is a term commonly used in the art and is clearly described in such a way as to enable one skilled in the art to make and/or use the claimed invention. As can be appreciated by those skilled in the art, and as evidenced in common textbooks and engineering manuals, the term is used to refer to a "high-output-impedance state." The term is clearly described in the specification and in accordance with its operational functionality. For instance, "the power signal Vcc is delivered to the output buffer 72, the drive controller 74, and the pad driver 76 to keep the I/O pad 78 in a tri-state condition during transition between modes." Page 12, lines 6-8. Further, "by 'tri-stating' the I/O pad 78 ... the power down state of the SRAM/DRAM chip 64 will not adversely effect other elements in the system." Page 12, lines 8-11. Still further, "the drive controller 74 is used to drive the output pad (or pads) 78 high, low, or into a tri-state condition." Page 12, lines 19-20.

Because the term "tri-state," as recited in the present claims, may be clearly understood by those skilled in the art, and because the Examiner has not presented any *evidence* to the contrary, Applicants respectfully submit that all of the terms recited in claim 12 are currently in

contrary, Applicants respectfully submit that all of the terms recited in claim 12 are currently in compliance with the requirements under 35 U.S.C. § 112, first paragraph. Accordingly, Applicants respectfully request withdrawal of the rejection under 35 U.S.C. § 112. If the Examiner chooses to maintain this rejection, Applicants are willing to provide an Affidavit, signed by a person of ordinary skill in the art, stating that the term is sufficiently descriptive so as to enable one skilled in the art to make and/or use the invention.

#### **Rejections Under 35 U.S.C. § 102**

The Examiner rejected claims 1 and 6-12 under 35 U.S.C. § 102(e) as being anticipated by Klughart (U.S. Pat. No. 6,396,137 B1). The Examiner also appears to be rejecting claim 5 as being anticipated by Klughart. Further, the Examiner appears to have taken Official Notice with regard to the subject matter recited in claims 2-4 and stated that the limitations claimed therein are well known in the art. If the Examiner maintains this rejection, Applicants respectfully request clarification of the rejection with regard to claims 2-5.

Applicants respectfully traverse this rejection. Anticipation under section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper

rejection under section 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984).

As a preliminary matter, Applicants respectfully submit that the rejection of claims 2-4 under 35 U.S.C. § 102 is improper. In the Official Action, the Examiner rejected claims 2-4 as being considered “well known in the art.” Applicants assume that the Examiner has taken Official Notice of facts outside of the record that the Examiner believes are “well-known” in the art. Because the Klughart reference is asserted against independent claim 1 and claims 2-4 depend from claim 1, Applicants assume that the Examiner has “combined” the Klughart reference with Official Notice to reject claims 2-4. However, the combination of multiple references is not a proper basis for rejecting a claim under 35 U.S.C. § 102. If the Examiner chooses to take Official Notice with regard to the subject matter recited in claims 2-4, Applicants respectfully request that a proper rejection be made.

Regardless, if the Examiner chooses to take Official Notice with regard to claims 2-4 and chooses to reject claims 2-4 based on a combination of Klughart and the Official Notice, Applicants respectfully traverse the rejection and challenge the Examiner’s use of the Official Notice in accordance with M.P.E.P. § 2144.03. Specifically, Applicants respectfully request that the Examiner produce evidence in support of the Examiner’s position, as well as a convincing line of reasoning as to why one of ordinary skill in the art would be motivated to combine any references cited.

With regard to independent claim 1, the Examiner stated:

Klughart discloses a system comprising: a processor (fig. 35, CPU 3523); a power supply coupled to the processor (fig. 35, power source 3501, col. 2, lines 16 – 17); and a device coupled to the processor and the power supply (fig. 35, 3503) and comprising: an internal power supply bus (fig. 35, 3505) configured to receive a power signal from the power supply; and an isolation (fig. 35, 3502) configured to disconnect internal power supply bus from the power supply by interrupting of the power signal (col. 38, lines 59 – 64).

The present application is directed to a technique of implementing a “zero power” standby mode with reduced leakage current. In operating electronic devices, a standby or sleep state is typically implemented to maintain power to certain components when the system is not in use. Typical electronic devices still exhibit some current leakage, even while they are in the standby or sleep state. Page 3, lines 15-22. To prevent or further reduce the leakage currents in this state, an isolation circuit, in accordance with the present invention, may be implemented within the system. Page 6, line 21 – page 7, line 3. The isolation circuit may be used to disconnect an internal power supply bus from the external voltage source to reduce leakage currents. Page 9, lines 3-8. Thus, the isolation circuit may be configured to reduce the leakage current and to provide a true “zero-power” standby mode.

Accordingly, independent claim 1 recites, a processor, a power supply coupled to the processor, and a device coupled to the processor and the power supply and comprising an internal power supply bus configured to receive a power signal from the power supply, and “an

isolation circuit configured to disconnect the internal power supply bus from the power supply by interrupting the flow of the power signal.”

Conversely, the Klughart reference is directed to an integrated voltage/current/power regulator/switch (VCPRS) system and method, wherein the regulator/switch circuitry is vertically integrated on top of an existing integrated circuit to reduce the on-resistance of the circuit. Abstract. The invention generally relates to the regulation and/or switching of voltage and/or current and/or power as applied to integrated circuits. Col. 1, lines 30-32. More specifically, the Klughart reference discloses a system for regulating the voltage of a microprocessor CPU 3523 by anticipating the load to be presented to the microprocessor CPU 3523. Col. 38, lines 44-53. To be clear, the reference merely discloses techniques for regulating the power demands of the microprocessor CPU 3523. Col. 39, lines 19-22.

In the rejection of claim 1, the Examiner cites the anticipatory switching/linear regulator subsystem 3503 as correlating to the “device” recited in claim 1. Further, the Examiner cites the high power demand signal 3505 as the “internal bus” of claim 1 and cites the integrated circuit 3502 as the “isolation circuit” recited in claim 1. As previously discussed, claim 1 recites a device comprising an internal power supply and an isolation circuit. However, it is clear from Fig. 35 of the Klughart reference that the switching/linear regulator subsystem 3503 can hardly be said to *comprise* either of the high power demand signal 3505 or the integrated circuit 3502

within the meaning of the terms. Conversely, the integrated circuit 3502 appears to comprise each of the switching/linear regulator subsystem 3503 and the high power demand signal 3505.

Furthermore, the integrated circuit 3502 is described in the Kughart reference as an existing integrated circuit, which is not utilized in the manner recited in the present application. Col. 16, lines 50-53. Indeed, as discussed above, the Klughart reference merely discloses a mechanism for regulating power demands in an integrated circuit 3502. There is nothing in the Klughart reference to suggest that the integrated circuit 3502 is “configured to disconnect the internal power supply bus from the power supply by interrupting the flow of the power signal,” as recited in claim 1. Accordingly, the integrated circuit 3502 cannot possibly comport with the subject matter of the rejected claims. In fact, there is nothing in the Kughart reference that is “configured to disconnect the internal power supply bus from the power supply by interrupting the low of the power signal.”

Accordingly, the cited reference fails to disclose *all* of the elements of the instant claims. Because the Examiner has failed to show that the cited reference discloses *all* of the claimed elements, the Examiner has failed to establish a *prima facie* case of anticipation, for at least the reasons discussed above. Accordingly, Applicants respectfully request withdrawal of the Examiner’s rejection and allowance of claims 1-12.

### **Conclusion**

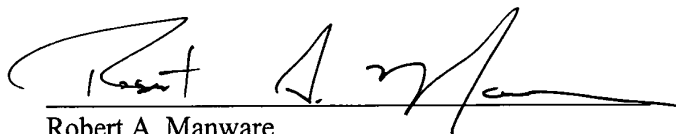
In view of the remarks and amendments set forth above, Applicants respectfully request withdrawal of the Examiner's rejections and allowance of claims 1-12. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

### **General Authorization for Extensions of Time**

In accordance with 37 C.F.R. § 1.136, Applicants hereby provide a general authorization to treat this and any future reply requiring an extension of time as incorporating a request therefor. Furthermore, Applicants authorize the Commissioner to charge the appropriate fee for any extension of time to Deposit Account No. 13-3092; Order No. MICS:0071/FLE (00-0901).

Respectfully submitted,

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